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GP2814

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Makoto Yamamoto

Serial No. 10/014,949

Filed: October 26, 2001

For: Lateral Transistor Having Graded Base Region,
Semiconductor Integrated Circuit And
Fabrication Method Thereof

#4A dmkt.
M. Brunson
7/22/02

) Art Unit: 2814

) Examiner: Shrinivas H. Rao

FIRST RESPONSE

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Responsive to the Office Action dated March 20, 2002 in the patent application identified above, please enter the following amendments and reconsider that application in view of the appended remarks.

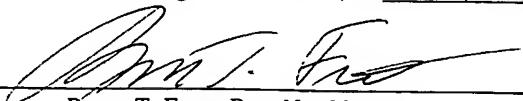
IN THE CLAIMS

Please amend Claims 1, 2, 5, 6, 8, 10 and 13 as follows:

1. (Amended) A lateral transistor comprising:
a semiconductor substrate of the first conductivity type;

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231, on June 20, 2002.


Roger T. Frost - Reg. No. 22,176

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